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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON
PORTLAND DIVISION

MEMORY INTEGRITY, LLC,	Case No. 3:15-cv-00262-SI
Plaintiff,	DEFENDANT INTEL CORPORATION'S SECOND NOTICE OF SUPPLEMENTAL EVIDENCE REGARDING CLAIM CONSTRUCTION
v.	
INTEL CORPORATION,	
Defendant.	

Intel respectfully submits this Second Notice of Supplemental Evidence pursuant to the Court's request during the claim construction hearing on March 11, 2016.

I. INTRODUCTION

Claim construction briefing in this case was completed on October 28, 2015. (*See* Dkt. 87 [Scheduling Order].) In its briefing, Memory Integrity relied on Dr. Daniel J. Sorin's textbook, "A Primer on Memory Consistency and Cache Coherence," to support its argument that the claim term "states associated with selected ones of the cache memories" in U.S. Patent No. 7,296,121 ("'121 patent") should be construed as "cache coherence protocol states associated with selected ones of the cache memories." (*See* Dkt. 135 [MI Opening Br.] at 33-34; Dkt. 139 [Jones Decl.] ¶¶ 31-32.) On November 28, 2015, after briefing was concluded but before the claim construction hearing in this matter, Dr. Sorin submitted a Supplemental Expert Declaration in an *inter partes* review proceeding before the Patent Trial and Appeal Board for the '121 patent. (*See Sony Corporation, Sony Electronics Inc., Sony Mobile Communications AB, and Sony Mobile Communications (USA) Inc. v. Memory Integrity, LLC*, IPR2015-00158, at Ex. Sony-1015.) As explained below and at the Claim Construction Hearing, Dr. Sorin's Declaration contradicts MI's position on the construction of the claim term "states associated with selected ones of the cache memories" and supports the construction proposed by Intel and tentatively adopted by the Court in its March 9, 2016 draft Opinion and Order on Claim Construction. (*See* Dkt. 192.)

II. DISCUSSION

Consistent with Intel's proposed construction of "states associated with selected ones of the cache memories," Dr. Sorin's Supplemental Expert Declaration explains that the claim term

"states" as used in the '121 patent includes information about presence—i.e., information about whether the requested data is or is not present in a particular location:

> The Patent Owner [MI] discusses several passages in this book and then proceeds to characterize the book by stating that "[t]his interchangeable use of the term 'states' and 'coherence states' and, use of the term 'state' alone to discuss the states of particular cache coherence protocol, demonstrates that the term 'state' means a cache coherence protocol state in the field of cache coherency." …. ***The Patent Owner's characterization of this book is overly restrictive***. While this book provides examples of various types of "states," ***it does not use the term "state" to mean only a cache coherence protocol state***. As examples, the book uses the terms "final states of the memory" and "state of a register." …. As used in these examples, ***the term "state" does not refer to a cache coherence protocol state***.

(Ex. 1 [Sorin Decl.] ¶ 19) (emphases added.[1])

> ***A person of ordinary skill in the art would understand the term 'states associated with selected ones of the cache memories' to not be limited to cache coherence protocol states, and be broad enough to include the condition of presence***—i.e., what is stored in cache memory. In fact, presence information alone (i.e., what is stored in cache memory), is enough information for maintaining coherence in a simple cache coherence protocol.

(*Id.* ¶ 17) (emphasis added).

[1] "Ex. 1" refers to the exhibit attached to the Declaration of Arthur W. Coviello in Support of Intel Corporation's Second Notice of Supplemental Evidence Regarding Claim Construction.

DATED this 14th day of March 2016.

By:

/s/ Renée E. Rothauge

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